In The Claims:

Claim 1. (currently amended) A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate;

forming a gate insulation layer and a conductive layer over the substrate sequentially;

performing a pre-amorphization implantation on the conductive layer so that the conductive layer is amorphized~~, wherein the pre-amorphization implantation is carried out using a dopant having an ionic radius greater than a germanium ion~~;

patterning the conductive layer and the gate insulation layer to form a gate structure;

forming a first spacer on the sidewalls of the gate structure;

forming a doped source/drain extension region in the substrate ~~on~~ aside each side of the first spacer;

forming a second spacer on the sidewall of the first spacer, meanwhile, performing a solid phase epitaxial process to re-crystallize the amorphized conductive layer in the gate structure and activating a plurality of first dopants in the doped source/drain extension region; and

forming a doped source/drain region in the substrate on each side of the second spacer~~;~~ ~~and~~

~~performing a solid phase epitaxial process to re-crystallize the amorphized conductive layer in the gate structure and activate the dopants in the doped source/drain extension region and the doped source/drain region to form a source/drain terminal~~.

Claims 2-4 (canceled)

Claim 5. (original) The method of claim 1, wherein a deposition temperature of a dielectric layer for forming the second spacer is in a range of 500°C~650°C.

Claim 6. (original) The method of claim 5, wherein the method for forming the second spacer comprise using a BTBAS (Bis(tert-butylamino)silane) as a precursor to carry out the deposition of the dielectric layer for forming the second spacer.

Claim 7. (original) The method of claim 1, wherein after the step of performing the pre-amorphization implantation, furthermore includes performing an ion implantation process to convert the conductive layer into an N-type or P-type conductive layer.

Claim 8. (currently amended) A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate having a gate structure thereon;

forming a first spacer on the sidewalls of the gate structure;

performing a pre-amorphization implantation to amorphize a portion of the substrate~~, wherein the amorphization implantation is carried out using a dopant having an ionic radius greater than a germanium ion~~;

forming a doped source/drain extension region in the substrate ~~on~~ aside each side of the first spacer;

forming a second spacer on the sidewall of the first spacer, meanwhile, performing a solid phase exitaxial process to re-crystallize the amorphized portion of the substrate and activating the doped source/drain extension region; and

forming a doped source/drain region in the substrate on each side of the second spacer~~;~~ ~~and~~

~~performing a solid phase epitaxial process to re-crystallize the amorphized portion of the substrate and activate the doped source/drain extension region and the doped source/drain region to form a source/drain terminal~~.

Claims 9-11 (canceled)

Claim 12. (original) The method of claim 8, wherein a deposition temperature of a dielectric layer for forming the second spacer is in a range of 500°C~650°C.

Claim 13. (original) The method of claim 12, wherein the method for forming the second spacer comprise using a BTBAS (Bis(tert-butylamino)silane) as a precursor to carry out the deposition of the dielectric layer for forming the second spacer.

Claim 14. (currently amended) A method of manufacturing a metal-oxide-semiconductor (MOS) transistor, comprising the steps of:

providing a substrate having a gate structure formed thereon, wherein the gate structure includes a gate insulating layer formed on the substrate, an amorphized gate formed on the gate insulating layer and a first pacer formed on a sidewall constructed by the gate insulating layer and the amorphized gate, and a portion of the substrate uncovered by the gate structure has been amorphized;

~~forming a gate insulation layer and a conductive layer over the substrate sequentially;~~

~~performing a first pre-amorphization implantation on the conductive layer so that the conductive layer is amorphized, wherein the first pre-amorphization implantation is carried out using a first dopant having an ionic radius greater than a germanium ion;~~

~~patterning the conductive layer and the gate insulation layer to form a gate structure;~~

~~forming a first spacer on the sidewalls of the gate structure;~~

~~performing a second pre-amorphization implantation on the substrate so that a portion of the substrate is amorphized, wherein the second pre-amorphization implantation is carried out using a second dopant having an ionic radius greater than a germanium ion;~~

forming a doped source/drain extension region in the substrate ~~on~~ aside each side of the first spacer;

forming a second spacer on the sidewall of the first spacer, meanwhile, performing a solid phase epitaxial process to re-crystallize the amorphized gate and the amorphized portion of the substrate and activating a plurality of first dopants in the doped source/drain extension region; and

forming a doped source/drain region in the substrate on each side of the second spacer~~;~~ ~~and~~

~~performing a solid phase epitaxial process to re-crystallize the amorphized conductive layer in the gate structure and the amorphized substrate and then activate the dopants in the doped source/drain extension region and the doped source/drain region to form a source/drain terminal~~.

Claims 15-20 (canceled)

Claim 21. (original) The method of claim 14, wherein a deposition temperature of a dielectric layer for forming the second spacer is in a range of 500°C~650°C.

Claim 22. (original) The method of claim 21, wherein the method for forming the second spacer comprise using a BTBAS (Bis(tert-butylamino)silane) as a precursor to carry out the deposition of the dielectric layer for forming the second spacer.

Claim 23. (canceled)

Claim 24. (new) The method of claim 1, wherein the pre-amorphization implantation is carried out by using a plurality of second dopants having an ionic radius greater than a germanium ion.

Claim 25. (new) The method of claim 24, wherein the second dopants comprise xenon, argon or krypton ions.

Claim 26. (new) The method of claim 24, wherein the pre-amorphization implantation is carried out using the second dopants set to a dosage level in a range of $1*10^{14}$ to $5*10^{14}$ atoms/cm^2.

Claim 27. (new) The method of claim 24, wherein the pre-amorphization implantation is carried out using the second dopants accelerated to an energy level in a range of 25 to 70 KeV.

Claim 28. (new) The method of claim 8, wherein the pre-amorphization implantation is carried out by using a plurality of first dopants having an ionic radius greater than a germanium ion.

Claim 29. (new) The method of claim 28, wherein the first dopants comprise xenon, argon or krypton ions.

Claim 30. (new) The method of claim 29, wherein the pre-amorphization implantation is carried out using the first dopants set to a dosage level in a range of $1*10^{14}$ to $5*10^{14}$ atoms/cm^2.

Claim 31. (new) The method of claim 29, wherein the pre-amorphization implantation is carried out using the first dopants accelerated to an energy level in a range of 25 to 70 KeV.